processed by said general processing module and said at least one specialized processing module.

28. (Amended) The system of claim 27, wherein said stream of input data is coupled with an associated timing [information] signal synchronized to a system clock signal, and each specialized processing module comprises a crosspoint switch which routes said stream of input data and its associated timing [information to/from respective] signal among the parallel pipelined hardware components, said timing [data compensating for pipeline delay in said specialized processing module] signal indicating when the input data represents active information.

29. (Amended) The system of claim 27, wherein said general processing module comprises at least two general purpose microprocessors and said hardware control library further comprises a set of functions for coordinating concurrent multitask processing operations of said at least two general purpose microprocessors.

30. (Amended) The system of claim 27, wherein said hardware control library includes [device information] control signals for each hardware component of said specialized processing system, wherein said functions of said hardware control library manipulate said [device information] control signals to program said hardware components for each of said different specialized processing operations.

REMARKS

Claims 1 through 30 are pending in the above identified application. All of the claims have been amended to more clearly define the invention and to more clearly define claim elements which had been inferentially claimed. No new matter has been added nor new issues raised.

Claims 1 and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nishitani. This ground for rejection is traversed because Nishitani et al.

does not disclose or suggest "A processing module containing at least one general purpose microprocessor" as set forth in claim 1. Nishitani et al. concerns a real time video signal processor which includes a plurality of signal processors connected in parallel between an input bus and an output bus. The system includes a control unit 300 as shown in Figure 25. As set forth at column 21, line 35, Figure 26 is a block diagram of the control unit 300. As shown in Figure 26, the control unit includes a row counter, a column counter, a plurality of read only memories and a plurality of AND gates. It does not include a microprocessor nor is any microprocessor which performs a control function disclosed by Nishitani et al. Because the Nishitani et al. does not include a control microprocessor, a necessary element of claim 1, it cannot anticipate claim 1. Accordingly, claim 1 is not subject to rejection under 35 U.S.C. §102(b) in view of Nishitani et al.

Similarly amended claim 20 includes the step of "connecting a processing module containing at least one general purpose microprocessor to said global video bus and said global control bus said microprocessor controlling hardware and software operations of said video processing system using control data and processing said video data." Basis for this amendment may be found in the specification in Figure 1 and in the specification at page 8, lines 13-17. Because the control unit of Nishitani et al. does not include a microprocessor it cannot describe a method of making a system which includes the step of connecting a processing module containing a microprocessor to a global databus. Accordingly, Nishitani et al. cannot anticipate claim 20 because the control unit is not coupled to the global data bus. Accordingly, claim 20 is not subject to rejection under 35 U.S.C. § 102(b) in view of Nishitani et al.

Claims 1 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wilson. Wilson discloses a single instruction multiple data (SIMD) parallel processor which employs a simple control function to allow a relatively large portion of the chip area to be devoted to signal processing circuitry. The subject invention is specifically not a SIMD system. A SIMD system issues a single instruction causing multiple processors to perform the same operation on different (multiple) data streams. The subject invention is, instead, a pipelined processor where each processor in a pipe performs a different instruction on the same data stream.

Furthermore, nothing in Wilson discloses or suggests that the controller 27 includes a microprocessor. Indeed, the presence of the host computer 25 would

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argue against the controller 27 including a microprocessor as there would be redundant functionality provided by the host computer 25 and controller 27.

In addition, Wilson discloses a shift register 21A through 21P which serially passes the received video data through each of the group of eight processing units 10a through 10n. This shift register is not connected to the controller 27. Thus, Wilson does not disclose a global video bus which allows data to be transferred between the processing unit and the video processing unit as required by claim 1. In the official Action, it is stated that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize well known techniques of distribution of video data along a common bus for the known benefit of synchronized delivery of data to a plurality of sources so that the data can be processed simultaneously." Applicants respectfully disagree with this assertion as Wilson teaches away from using a video bus which distributes the data along a common bus. Specifically, at column 2 lines 5 through 43, Wilson teaches that if the memory is outside of the integrated circuit, which Wilson sees as desirable, and conventional methods such as a data bus were used to assign the data to a particular processor, then "there [would be] too many address lines that the processors must handle, so that the number of signal paths is a strong limiting factor." Thus, a central feature in the Wilson system is the serial shift register through which data are transferred sequentially among the processing elements to minimize addressing circuitry and to minimize the number of off-chip connectors.

In addition, at column 2 lines 21 through 27, Wilson states:

> [U]sually a memory write inhibit function is used where a programmable flip flop controls the write function for each memory in the array. However, the write inhibit function requires an extra line from the processor chip to the associated memory chip. Because of output pin limitations on the circuit chips, not too many processors can be integrated on a single chip.

If Wilson were to use a global video bus as disclosed in this subject patent application, each of the separate processors in Wilson would need to separately provide addresses, perhaps to a common address bus or directly to separate off-chip memories, to address the memories which provide data to the global memory bus. If a common address bus is used then, because the Wilson system is SIMD, it would also require logic to resolve conflicting address requests and each of the signal processors would need circuitry to

suspend execution until all processors have filled their address spaces. As set forth in the quoted passages above, this is contrary to Wilson's motivation of maximizing the amount of area on the chip that is dedicated to processors and minimizing the area devoted to overhead functions. Thus, viewing the reference as a whole, Wilson teaches away from using a global data bus.

Claim 20 includes similar limitation. Because Wilson does not disclose of suggest a global data bus, a processing module which includes a microprocessor or a microprocessor which performs both control and data processing functions, these claims are not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson.

Claims 2 through 3, 17 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wilson in view of McMullen, Jr. et al. This ground for rejection is respectfully traversed. Wilson is described above. McMullen, Jr. et al. concerns a digital transmission system which uses a crosspoint switch to selectively couple a plurality of video channels to a plurality of encoders. As set forth above, Wilson discloses an SIMD processing system. It is inherent in an SIMD processing system that a single instruction set and multiple data sets are used such that each processor in the SIMD system is operating in lock step, on the same instructions at the same time, but on a different data set. The relationships among the data sets in a particular algorithm does not change therefore there would be no need in Wilson for a cross-point switch as disclosed in McMullen, Jr. et al. Indeed, as set forth above, Wilson teaches away from such a combination at column 2, lines 5 through 43 where he states that it is undesirable to have extra off chip connectors to supply data to the parallel processors.

Thus, a person of ordinary skill in the art who had knowledge of both Wilson and McMullen, Jr. et al. would not be motivated to combine them to include a crosspoint switch in the SIMD processing system disclosed by Wilson because a crosspoint switch has no use in a SIMD processor and because to do so would go against the teachings of Wilson. Indeed, the only motivation to combine Wilson with McMullen, Jr. et al. comes from Applicants own disclosure. Thus, Applicants' disclosure is being used against them. It is well settled that this method of invalidating a claim is improper.

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge

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> generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.* (emphasis added)[1]

Because neither Wilson nor McMullen, Jr. et al. disclose a global data bus connected to a control microprocessor, a processing module which includes a microprocessor, or a cross-point switch which interconnects the hardware devices of the video processing module, claims 2 through 3, 17 and 19 are not subject to rejection under 35 U.S.C. §103(a) as being unpatentable in view of Wilson and McMullen, Jr. et. al.

In addition, claims 2 and 3 are not subject to rejection under 35 U.S.C. §103(a) in view of Wilson and McMullen, Jr. et al. because neither Wilson, McMullen, Jr. et al. nor any combination thereof disclose or suggest that the "video data is coupled with associated video timing signals, ... said timing signals indicating when the video data represents active video information," as set forth in amended claim 2. Basis for this amendment may be found in the specification at page 12, line 29 through page 14, line 7.

Wilson does not disclose any timing signals associated with the data signals. In Wilson, the video data are applied to a serial shift register which shifts through the various video processors to produce an output data stream. There is no indication in Wilson that any timing information is associated with the data signals. Indeed, it appears that the timing of the signals is determined by the host computer 25 as the host computer provides the controlling signals 26 to the controller 27 which provides the "clock and control signals" to the processor unit groups 10a-10n via control lines 29. (see col. 6, lines 13-33).

McMullen Jr. et al. concerns a signal switching system which does not disclose or suggest any video processing or any applicability to video signal processing. As set forth above, McMullen Jr. et al. was combined with Wilson based only on the disclosure of a crosspoint switch from the subject patent application. Accordingly, McMullen Jr. et al. does not correct the defect in Wilson.

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[1] MPEP §706.02(j)

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Furthermore, amended claim 3 is not subject to rejection in view of Wilson and McMullen Jr. et al. because neither Wilson, McMullen, Jr. et al. nor their combination discloses or suggests a crosspoint switch state machine "which monitors transfers of video data over each data path of said crosspoint switch and allocates paths for transferring the video data among the parallel pipelined video hardware components." Basis for this amendment may be found at page 15, line 10 through page 16, line 19. McMullen, Jr. et al. does not disclose or suggest a crosspoint switch state machine. All paths through the crosspoint switch are allocated by the external computer 135 (see col. 8, lines 55 through 61). Because the computer 135 of McMullen, Jr. et al. controls the entire switching operation and because there are no independent operations which route data through the crosspoint switch, McMullen, Jr. et al. cannot disclose or suggest a crosspoint switch state machine as claimed in claim 3.

Because neither Wilson nor McMullen, Jr. et al., either alone or in combination, discloses or suggests associating timing signals with the video signals in a video signal processing system, claim 2 is not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson and McMullen, Jr. et al. Claim 3 depends from claim 2 and is not subject to rejection under 35 U.S.C. § 103(a) for at least the same reasons as claim 2.

Claims 17 and 19 are not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson and McMullen, Jr. et al. because neither Wilson nor McMullen, Jr. et al. disclose or suggest "a set of functions for programming the parallel pipelined video hardware of said at least one video processing module to perform respective ones of said different video processing operations *concurrently*," as set forth in amended claim 17. Basis for this amendment may be found in the specification at page 29, line 29 through page 30, line 6.

As described above, Wilson concerns a single instruction multiple data (SIMD) video processing system. By definition, such a system operates the video processors in lock-step; all processors perform the same instructions at the same time but on different data sets. Accordingly, Wilson has no need for "a set of functions for programming the parallel pipelined video hardware of said at least one video processing module to perform respective ones of said different video processing operations concurrently." McMullen Jr. et al. was only disclosed for its crosspoint switch. McMullen Jr. et al. does not disclose or suggest any video processing and, so, can not correct the defect in Wilson. Because neither Wilson nor McMullen et al.

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either alone or in combination discloses or suggests this element of claim 17, claim 17 is not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson and McMullen et al. Claim 19 depends from claim 17 and is not subject to rejection under 35 U.S.C. § 103 in view of Wilson and McMullen et al. for at least the same reasons as claim 17.

Claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Wilson, McMullen, Jr. et al. and Suzuki et al. Suzuki et al. discloses a multi-processor system having a programmable memory-access priority control system. Because Suzuki et al. does not disclose or suggest any video processing, it cannot disclose or suggest "a set of functions for programming the parallel pipelined video hardware of said at least one video processing module to perform respective ones of said different video processing operations concurrently," as set forth in claim 17 from which claim 18 depends. Accordingly, claim 18 is not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson, McMullen, Jr. et al. and Suzuki et al. for at least the same reasons as claim 17.

In addition, none of Wilson, McMullen, Jr. et al. nor Suzuki et al. disclose or suggest a "hardware control library further [comprising] a set of functions for coordinating concurrent multitask processing operations of said at least two general purpose microprocessors," as set forth in amended claim 18. Basis for this amendment may be found at page 29. line 29 through page 30, line 20. Wilson and McMullen are described above. Neither Wilson nor McMullen Jr. et al. disclose or suggest multiple microprocessors. Suzuki et al. discloses a programmable memory access controller which selectively allows only one of CPU#1, CPU#2 and the DMA channel to access the shared memory at any one time. (See column 2, lines 1-26). Because Suzuki et al. disclose that only one operation can occur at any one time, there can be no "concurrent multitask processing operations" as required by claim 18. Accordingly, claim 18 is not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson, McMullen Jr. et al. and Suzuki et al.

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Wilson, McMullan Jr. et al. and van der Wal. Claim 5 depends from claim 1. As set forth above, neither Wilson nor McMullan Jr. et al. disclose or suggest "a processing module containing at least one general purpose microprocessor, which controls hardware and software operation of said video processing system using control data, and which processes video data," as set forth in claim 1. The van der Wal patent concerns a pyramid processor which is used as a component of the subject invention. van der Wal does not disclose or suggest "a processing module containing at least one

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general purpose microprocessor, which controls hardware and software operation of the video processing system using control data, and which processes video data." Accordingly, claim 5 is not subject to rejection under 35 U.S.C. § 103 in view of Wilson, McMullan, Jr. et al. and van der Wal.

In addition, there is no suggestion in Wilson, McMullan, Jr. et al. nor van der Wal that would support their combination. The only such suggestion comes from the subject application. Thus, Applicants' own disclosure is impermissibly being used against them. In the Official Action it is asserted that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Wilson and McMullan to include pyramid processing of video data at different resolutions as taught by van der Wal, for the well know benefit of improving the results of image processing by filtering images according to their resolution." Applicants respectfully disagree with this assertion because Wilson discloses a SIMD processor and, thus, the pyramid processor would need to be implemented in a SIMD environment. The amount of change required to the Wilson system would be prohibitive. As disclosed, Wilson receives the video data via a shift register and provides output signals via the same shift register. It is unclear how pyramid processing, which is necessarily block oriented, could proceed in the Wilson system. As set forth above, the likelihood of success in implementing a proposed combination cannot be ignored in determining whether the combination would render an invention obvious.

Claims 6-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Wilson, McMullen, Jr. et al. and Conroy-Wass et al. Wilson and McMullen, Jr. et al. are described above. Conroy-Wass et al. concerns a printed circuit board mounting cage which has orthogonal slots to allow one motherboard to receive a plurality of daughter boards. (See col. 3, lines 50-59). Because Conroy-Wass does not correct the defects in Wilson and McMullen, Jr. et al. noted above with respect to claims 1 and 2 from which claim 6 depends, claim 6 is not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson, McMullen, Jr. et al. and Conroy-Wass et al. In addition the combination of Wilson, McMullen, Jr. et al. and Conroy-Wass et al. does not disclose or suggest a "modular video processing system [that] includes a plurality of video processing modules and each video processing module comprises a connection for at least one daughterboard," as required by amended claim 6. Basis for this amendment may be found in the specification in Figure 1 which shows two video processing modules 20, each including two video

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processing daughterboards. Conroy-Wass, by contrast, discloses a single motherboard having a plurality of daughterboards. Furthermore, it is difficult to determine how Conroy-Wass may be modified to meet the limitations of claim 6.

Finally, the only suggestion to combine Conroy-Wass with Wilson and McMullen, Jr. et al. comes from Applicants' own disclosure. Accordingly, once more, Applicants' disclosure is impermissibly being used against them. For the reasons set forth above, claim 6 is not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson, McMullen, Jr. et al. and Conroy-Wass. Claims 7-9 depend from claim 6 and are not subject rejection under 35 U.S.C. § 103(a) in view of Wilson, McMullen, Jr. et al. and Conroy-Wass for at least the same reasons as claim 6.

Claims 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wilson, McMullen, Jr. et al., Conroy-Wass and Bruehl et al. Wilson, McMullen, Jr. et al. and Conroy-Wass are described above. Bruehl et al. relates to a system for processing video images derived from film. It was cited solely for the proposition that it was known to include an image warper in a video signal processing system. This ground for rejection is traversed as follows. Bruhel does not disclose or suggest 1) a processor module which includes a microprocessor that both provides control signals and processes video data 2) timing signals that are associated with video data, 3) a crosspoint switch, and 4) multiple video processing modules, each including at least one daughterboard connection. As set forth above, none of these elements of claims 10 and 11 is disclosed in any of the other references: Wilson, McMullen, Jr. et al. and Conroy-Wass. Accordingly, claims 10 and 11 are not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson, McMullen, Jr. et al., Conroy-Wass and Bruehl et al.

Claims 12-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Wilson and Suzuki et al. This ground for rejection is traversed as follows. As set forth above, there is no suggestion in Wilson that the controller 27 includes a microprocessor. Indeed, because of the host computer 25, it would be unnecessary to include a microprocessor in the controller 27. Furthermore, because Wilson describes a SIMD processor, there would be no need for two microprocessors. SIMD processors operate on a single broadcast instruction set, thus, there is no need to have two microprocessors to send the one instruction set. Furthermore, neither Wilson nor Suzuki et al. either alone or in combination discloses or suggests a processor module having at least two microprocessors, each having a memory which is not shared. Wilson does not describe a microprocessor in the controller and, so, can

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not describe two microprocessors. Furthermore, Suzuki et al. does not describe any non-shared memory. In addition, Suzuki et al. does not concern video processing and the only suggestion to combine Wilson with Suzuki et al. comes from Applicants' own disclosure. Therefore, Applicants' disclosure is improperly being used against them.

Furthermore, claim 13 is not subject to rejection under 35 U.S.C. §103(a) in view of Wilson and Suzuki et al. because neither of these references either alone or in combination discloses or suggests the use of a "synchronous start signal to begin the at least one video processing operation" as set forth in claim 13. As set forth above, because the Wilson system is an SIMD processor, it has no need for such a synchronous start signal, because all of the processors operate in lock-step, all of the data will be ready at the same time.

In addition, claim 14 is not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson and Suzuki et al. because neither of these references either alone or in combination discloses or suggests "a communications interface for communicating with external devices, said communications interface being coupled to said arbitrated control bus for access by each of said at least two microprocessors," as set forth in amended claim 14. Basis for this amendment may be found in items 334 and 340 of Figure 4. While Suzuki et al. does disclose multiple processors accessing a shared memory, it does not indicate that a communications interface may be accessed in the same manner.

Claim 15 is not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson and Suzuki et al. because neither of these references either alone or in combination discloses or suggests that the "random access memory associated with each microprocessor is connected to said global video bus to store video data for transmission to, and video data received from said at least one video processing module over said global video bus." As set forth above, the video data in Wilson is transferred using a shift register which is not connected to the controller. In addition, none of the references discloses or suggests a controller having a local memory that is coupled to a global video bus.

For the reasons set forth above, claims 12-15 are not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson and Suzuki et al.

Claim 16 was rejected under 35 U.S.C. § 103(a) in view of Wilson, Suzuki et al., and Charles et al. This ground for rejection is traversed as follows. Wilson and Suzuki et al. are described above. Charles et al. concerns a processing

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system which utilizes multiple clock signals. It was cited for the proposition that semaphores were known. Claim 16 is not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson, Suzuki et al., and Charles et al. because none of these references, either alone or in combination discloses or suggests, 1) a processor module including a microprocessor which both controls video processors and processes video data, 2) at least two microprocessors, each having a non-shared memory, and 3) a semaphore register which is available to the at least two microprocessors via an arbitrated control bus. While Charles et al. does disclose semaphores, there is no indication in Charles et al. that the semaphore register may only be accessed via an arbitrated control bus. In addition, the only suggestion to combine Charles et al. with Wilson and Suzuki et al. comes from Applicants' own disclosure. Accordingly Applicants' disclosure is improperly being used against them. For the reasons set forth above, claim 16 is not subject to rejection under 35 U.S.C. § 103(a) in view of Wilson, Suzuki et al., and Charles et al.

Claims 1 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Chau. This ground for rejection is traversed because, with the possible exception of the global control bus, Chau does not disclose or suggest any of the elements of claims 1 and 20. Chau concerns a microprogrammed control system. There is no indication in Chau that video data is processed. While Figure 7 of Chau shows an application of the Chau controller in an MPEG decoder, it is well known that MPEG decoders decode digitally coded signals to reproduce images. Typically no signal processing is performed. Chau does not disclose a processor module which includes a microprocessor. Chau's system includes next program counter logic, a microprogram memory storage and a micro instruction register. None of these nor all of these would qualify as a microprocessor. A microprocessor, at a minimum, also includes an arithmetic and logic unit. In addition, the microprocessor is not coupled to a global video data bus. No global video data bus can exist in the MPEG decoder because video data is only available at the output of the decoder. Chau does not disclose or suggest any video processing modules. The "functional units" disclosed in Figure 7 may be variable length decoders and inverse discrete cosine processors which convert MPEG encoded data into video data but they do not process the video data in any of the ways disclosed in the subject patent application. This ground for rejection is based on supposition and inference gained from Applicants' own disclosure. Again, Applicants' disclosure is impermissibly being used against them.

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Because Chau only arguably includes one element from claim 1, it cannot disclose or suggest the elements of claim 20 which concern the method of assembling the elements of claim 1. For the reasons set forth above, claims 1 and 20 are not subject to rejection under 35 U.S.C. § 103(a) in view of Chau.

Claims 1 and 20 were rejected under 35 U.S.C. § 103(a) in view of Toyoda et al. This ground for rejection is overcome by the amendments to claims 1 and 20. In particular, Toyoda et al. do not disclose or suggest "a processing module containing at least one general purpose microprocessor which controls hardware and software operation of said video processing system using control data and which processes video data," as set forth in claim 1 or the step of "connecting a processing module containing at least one general purpose microprocessor to said global video bus and said global control bus said microprocessor controlling hardware and software operations of said video processing system using control data and processing said video data," as set forth in claim 20. In Toyoda et al., the control means 105 is connected to the bus means only to provide control signals. It is not connected to receive or process video data that may be applied to the bus means. Having the microprocessor coupled to the video data bus to both to process video data and control the processing of video data by other processing elements gives the subject invention a distinct advantage over the apparatus disclosed by Toyoda et al. Because Toyoda et al. does not disclose or suggest elements of claims 1 and 20, Claims 1 and 20 are not subject to rejection under 35 U.S.C. §103(a) in view of Toyoda et al.

Claims 2, 4, 20-22, 24-28 and 30 are rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Toyoda et al. and McMullen, Jr. et al. This ground for rejection is overcome by the amendments to claims 1 and 20. As described above, Toyoda et al. does not disclose or suggest at least one element in each of claims 1 and 20. Claim 27 includes similar limitations and is not subject to rejection under 35 U.S.C. § 103(a) in view of Toyoda et al. for at least the same reasons as claims 1 and 20.

As set forth above, McMullen, Jr. et al. was cited only for the proposition that crosspoint switches were known. McMullen, Jr. et al. does not disclose or suggest any signal processing and, thus, cannot disclose or suggest a microprocessor that performs both control functions and signal processing functions. Furthermore, There is no suggestion, except for Applicants' disclosure, that would support the combination of McMullen, Jr. et al. with Toyoda et al. Accordingly, in

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making the combination, Applicants' own disclosure is improperly being used against them.

Claims 2 and 4 depend from claim 1, claims 21-26 depend from claim 20 and claims 28 and 30 depend from claim 27. These claims are not subject to rejection in view of Toyoda et al. and McMullen, Jr. et al. for at least the same reasons as their base claims.

Considering claims 2, 4 and 26, Toyoda et al. do not disclose or suggest associating timing signals with the video data such that the timing signals indicate when the video data represents active video signals.

Considering claim 22, in the Official Action it is asserted that "the step of providing at least one synchronous start signal to the video processors is necessarily included in Toyoda, as it is disclosed that the video processors are synchronized." Applicants' respectfully disagree with this assertion. There are many other ways of synchronizing processors than issuing a synchronous start signal. Processors may, for example, be synchronized by simply having a common clock signal. Toyoda et al. do not disclose or suggest any synchronous start signal which would conform to the start signal as claimed in claim 22.

Considering claim 24, as set forth above, McMullen, Jr. et al. do not disclose or suggest any crosspoint switch state machine which monitors transfers through the switch and allocates paths through the crosspoint switch. In McMullen, Jr. et al., all path allocation is done, at a global level, by the computer 135 (see column 8, lines 55-56). As set forth above, the subject invention achieves significant advantages by controlling the crosspoint switch using the crosspoint switch state machine. These advantages would not be realized by the configuration disclosed in McMullen, Jr. et al.

Claims 23 and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Toyoda et al., McMullen, Jr. et al. and Muramatsu. This ground for rejection is traversed as follows. First, claim 23 depends from claim 20 and claim 29 depends from claim 27. Muramatsu discloses a multiprocessor system having an offset address setting. Muramatsu does not disclose or suggest any signal processing operations being performed by the multiprocessors. Accordingly, Muramatsu does not correct the defects in Toyoda et al. and McMullen, Jr. et al., as described above with reference to claims 20 and 27.

Second, Toyoda et al. describe a fully synchronous system in which data from processor 101 is provided only to processor 102 and data from processor 102 is

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provided only to processor 103 (see Figure 2). Thus, the Toyoda et al. system can only perform one function at a time using all three processors. Consequently, Toyoda et al. have no need for multiple microprocessors. Because neither Toyoda et al. nor McMullen, Jr. et al. would benefit from having multiple control microprocessors, the suggestion to combine Toyoda et al., McMullen, Jr. et al. and Muramatsu can only come from Applicants' own specification. Once again, Applicants' specification is impermissibly being used against them.

For the reasons set forth above, claims 23 and 29 are not subject to rejection under 35 U.S.C. § 103(a) in view of Toyoda et al., McMullen, Jr. et al. and Muramatsu.

In view of the foregoing amendments and remarks, Applicants respectfully request that the rejection of claims 1-30 be reconsidered and withdrawn and that claims 1-30 be passed to allowance.

Respectfully Submitted,

Kenneth N. Nigon, Reg. No. 31,549
Attorney for Applicant

KNN/mm
Dated: June 1, 1999

Sarnoff Corporation
201 Washington Road
CN5300
Princeton, NJ 08543-5300
(609) 734-2454

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